Office Action Summary	Application No.	Applicant(s)	
	10/614,558	JONES, DAVID E.	
	Examiner	Art Unit	
	Hicham B. Foud	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/02/2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 07-02-2007 has been entered and considered.

Claims 1-25 are pending in this application.

Claims 1-25 remain rejected as discussed below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 7, 12, 14, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Toda et al (5,612,925).

For claim 1, Toda et al discloses a packet buffer random access memory (PBRAM) device, comprising: (a) a memory array (see figure 16 element 162 wherein the is arranged by cell group); (b) a plurality of input ports to be coupled to a network controller device (see Figure 16 element 164, I/O section is coupled to a control section which is element 166), the memory array for storing packet data received by the plurality of input ports being shared by the plurality of input ports (see figure 16, element 164 wherein data is shared by I/O); and (c) a plurality of serial registers associated with the input and output ports (see Figure 16 element 164 is connected to I/O), the serial registers simultaneously receiving packet data from the input ports and writing packet

data to the memory array (see Figure 16, wherein the connection between the I/O and serial registers and the memory cell group), the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array(see Figure 16 wherein the section 164 is segmented to a plurality of segments that are associated to a corresponding memory cell group), segments of different serial registers simultaneously transferring packet data to different portions of the memory array (see column 12 lines 8-12).

For claim 2, Toda et al discloses a packet buffer random access memory (PBRAM) device wherein packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register (see Figure 16, the connection between the I/O, serial registers and the memory and see column 12 lines 8-12).

Claim 7 is rejected for same reasons as claim 1, since claim 7 is the method carried out by the system of claim 1.

For claim 12, Toda et al discloses a packet buffer random access memory (PBRAM) device comprising: a memory array (see figure 16 element 162 wherein the is arranged by cell group); a plurality of input ports coupled to the memory array by serial registers for conveying data to the memory array (see Figure 16 element 164 is connected to I/O which is element 164), the memory array for storing packet data received by the plurality of ports being shared by the plurality of input ports (see Figure 16, wherein the connection between the I/O and serial registers and the memory cell group); a plurality of command ports for receiving commands that indicate desired

operations to be performed in relation to the data conveyed on the input and output ports (see Figure 16, wherein the element 166 which is control section send commands to the data section to perform the desired operations); and a memory management unit coupled between the command ports and the memory array (see Figure 16, elements 163, 168 and 165), the memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports (see figure 16, wherein element 163 is connected to the control section 166), the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports (see figure 16, element 163 which comprises of addresses of the data in the memory and designates the memory cells which are to be accessed (see column 5 lines 11-15)).

For claim 14, Toda et al discloses a method for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising the steps of: receiving a packet from a controller coupled to the computer network by one of a plurality of input ports of the PBRAM device (see figure 16, element 164 wherein data is shared by I/O); storing the packet in a physical location of a memory array of the PBRAM device (see figure 16, element 162 wherein data is stored), the memory array being shared by the plurality of input ports (see figure 16, element 164 wherein data is shared by I/O); storing a pointer to the physical location in an entry of a packet table in the memory array (see figure 16, element 162 wherein data is stored); storing a pointer to the entry in the packet table in an input queue structure, contained in the memory array of the PBRAM device (see figure 16, element 163 which

comprises addresses of the data in the memory and designates the memory cells which are to be accessed (see column 5 lines 11-15)); and the input queue structure being further accessible by a plurality of output ports of the PBRAM device such that the pointer in the input queue structure is transferred to an associated output queue structure (see Figure 16 wherein element 163 is connected to I/O (element 164) through the control section (element 166) and the addresses of the data stored in the memory is inherent to the pointers are in the element 163 which is considered both input and output queue).

For claim 18 and 22 are rejected for same reasons as claims 7 and 14, since claims 18 and 22 are the apparatus carried out by the method of claim 7 and 14.

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 11, 13, 17, 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda et al.

For claims 6, 11, 13, 17, 21 and 25 are rejected because it would have been obvious over the claimed invention of Toda et al to have the memory array as a single global memory. The difference between the memory array as taught by the invention of Toda et al and the single global memory is that the memory array is a specific arrangement of memory that can be depending on different factors such as data type, and the single global memory is a regular memory that holds all data without any specific arrangement. Therefore, an official notice is taken in that a memory array can be arranged as a single global memory. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to have the memory array as a single global memory. The motivation of having the memory array as a single global memory is being that it allows all the stored data in the memory available to all the ports and for simplicity.

5. Claims 3-5, 8-10, 15, 16, 19, 20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda et al in view of Zuravleff et al (5,867,735).

For claims 3-5, 8-10, 15,16, 19, 20, 23 and 24, Toda et al discloses all the subject matter with the exception of wherein a portion of the memory array is a queue, the queue includes a plurality of sub-queues and each sub-queue assigned a priority level wherein packet data is read from the sub-queue with the highest priority level that stores data. However, the invention of Zuravleff et al from the same or similar fields of

endeavor shows that a portion of the memory array is a queue (see column 6 lines 65-66, wherein elements 114 are queues), the queue includes a plurality of sub-queues (see column 10 lines 25-27, wherein elements 114 are divided to elements 214 which are subqueues) and each sub-queue assigned a priority level (see column 10 lines 31-32 wherein each subqueue has a unique priority level) wherein packet data is read from the sub-queue with the highest priority level that stores data (see column 10 lines 39-42 wherein the highest priority level subqueues are read first). Thus, it would have been obvious to the person of ordinary skill in the art at the time of invention to use the division of queues to subqueues and the method of priority level of subqueues as taught by the invention of Zuravleff et al in the invention of Toda et al. The motivation of having a portion of the memory array as a queue, wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level and wherein packet data is read from the sub-queue with the highest priority level that stores data is being that is gives a good arrangement to the memory for easier function by dividing a queue to a plurality of sub-queues, and read the packet data that were stored in subqueues which are assigned a highest priority level to them before any other subqueues to reduce the effect of memory latency.

Response to Argument

6. Applicant's arguments filed have been fully considered but they are not persuasive.

In page 9 lines 27-30, the applicant argues that Toda does not disclose a plurality of inputs and that he merely discloses a single I/O port 164 that sends and receives

data serially. However, the examiner respectfully disagrees with the applicant because Toda does not specify that the I/O section 164 is a single I/O port because in Toda's invention the number of input/output ports is irrelevant since the plurality of input ports can be connected through a data bus or an interface that combines the data coming from the plurality of input ports and output them serially as taught by the invention of Balmforth et al (US 5,187,795) in Figure 1 wherein the plurality of input ports are connected through the interface 11 and called I/O section (see column 4 lines 11-14).

In page 10 lines 2-5, the applicant argues that Toda does not disclose a plurality of serial registers, however the examiner respectfully disagrees with the applicant because Toda discloses on column 12 lines 18-19 that a serial register section 167 comprising a plurality of serial registers.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hicham B. Foud whose telephone number is 571-270-1463. The examiner can normally be reached on Monday - Thursday 10-3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hicham Foud

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600